

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO. 501.33873VC4	SERIAL NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT KAWAGOE, et al.	
		FILING DATE December 14, 2001	GROUP 5

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## U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
AA	4,835,740	5-89	Sato			
AB	5,290,714	3-94	Onozawa			
AC	4,761,384	8-88	Neppl			
AD	5,156,990	10-92	Mitchell			
AE	6,043,114	3-00	Kawagoe			
AF	4,564,416	1-86	Homma, et al.			
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AJ	5,508,540	4-96	Ikeda, et al.			
AK	5,508,549	4-96	Watanabe, et al.			
AL	3,974,003	8-76	Zirinsky, et al.			

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Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation /Abstract	
						Yes	No
AM	0373723	6-20-90	Europe				
AN	0550021	7-85	Europe				
AO	60132358	7-85	Japan				
AP	58218159	12-83	Japan				
AQ	63157477	6-88	Japan				
AR	61002356	1-86	Japan				
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AV	AU	Wolf, S., "Silicon Processing for the VLSI Era Vol. 1", ppg. 64-65.
AV	AV	Ghandhi, S., "VLSI Fabrication Principles Silicon and Gallium Arsenide", ppg. 735-738.
AV	AV	Yamaguchi, et al., "Process integration and device performance of a submicrometer BiCMOS with 16-GHz fT double Poly-Bipolar devices", IEEE Transactions on Electron Devices, Vol. 36, No. 5, ppg. 890-896.
	AX	
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	AZ	

Examiner	Date Considered
<i>Bob J. Hs</i>	6/14/01

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AC	4,717,686	1-88	Jacobs, et al.			
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